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IN THE CLAIMS:

1. (Amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) forming an insulating film above said MISFET by the plasma CVD method at a temperature of 450°C to 700°C;

(c) forming a trench by etching said insulating film;

(d) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said insulating film to leave the silicon film only on an inner surface of said trench;

(e) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(f) forming a dielectric film on said rugged surface silicon film and on said insulating film and forming a plate electrode on said dielectric film.

2. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said rugged surface silicon film is formed by crystal grains which are grown from crystal nucleuses of silicon deposited on said silicon film.

Q1

Please cancel Claims 3, 7, 9, and 13 without prejudice.

4. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

Q2

wherein said semiconductor integrated circuit device has a first area in which said memory cell is formed and a second area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

(e) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

5. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said plasma CVD method is a high-density plasma CVD.

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6. (Amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell including a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a first temperature;

(c) depositing a second insulating film on said first insulating film at a second temperature between 450°C and 700°C that is higher than said first temperature;

(d) forming a trench by etching said first and second insulating films;

(e) depositing a silicon film on said second insulating film and in said trench, and removing the

silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

(f) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(g) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

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10. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 6,

wherein said semiconductor integrated circuit device has a first area in which said memory cell is formed and a second area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

(h) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate

electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

11. (Amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate;

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(b) forming an insulating film containing impurity above said MISFET by a high density plasma CVD method at a temperature of 450°C to 700°C;

(c) forming a trench by etching said insulating film;

(d) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said insulating film to leave the silicon film only on an inner surface of said trench;

(e) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of a capacitor on the inner wall of the trench; and

(f) forming a dielectric film on said rugged surface silicon film and on said insulating film and forming a plate electrode on said dielectric film.

14. (Amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a first temperature;

(c) planarizing a surface of said first insulating film;

(d) forming a second insulating film containing impurity on said first insulating film at a second temperature higher than said first temperature;

(e) forming a trench by etching said first and second insulating films;

(f) depositing a silicon film on said second insulating film and in said trench, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

(g) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of a capacitor on the inner wall of the trench; and